WHAT IS CLAIMED IS:

1. A byte execution unit, comprising:

logic coupled to receive byte instruction information and two operands and configured to perform an operation specified by the byte instruction information upon at least one of the two operands, thereby producing a result, wherein the byte instruction specifies either a count ones in bytes operation, an average bytes operation, an absolute differences of bytes operation, or a sum bytes into halfwords operation.

2. The byte execution unit as recited in claim 1, wherein each of the two operands comprises a plurality of bits, and wherein the bits of the two operands are grouped to form a plurality of corresponding 8-bit bytes.

3. The byte execution unit as recited in claim 2, wherein each of the two operands comprises 128 bits, and wherein the bits of the two operands are grouped to form 16 corresponding bytes.

4. The byte execution unit as recited in claim 2, wherein in the event the byte instruction information specifies the count ones in bytes operation, the byte execution unit is configured to count a number of logic one bits in each of the bytes of one of the two operands, and wherein the result is indicative of the number of logic one bits in each of the bytes.

5. The byte execution unit as recited in claim 2, wherein in the event the byte instruction information specifies the average bytes operation, the byte execution unit is configured to compute averages of corresponding bytes of the two operands, and wherein the result is indicative of the averages.

6. The byte execution unit as recited in claim 2, wherein in the event the byte instruction information specifies the absolute differences of bytes operation, the byte execution unit is configured to subtract a value of a byte of one of the two operands from a value of a corresponding byte of the other operand, and to compute an absolute value of

a result of the subtraction operation, and wherein the result is indicative of the absolute value of the result of the subtraction operation.

7. The byte execution unit as recited in claim 2, wherein in the event the byte instruction information specifies the sum bytes into halfwords operation, the byte execution unit is configured to compute sums of values of a number of consecutive bytes of the two operands, and wherein the result is indicative of the sums.

8. A byte execution unit, comprising:

pre-processing logic coupled to receive a plurality of operands and configured to perform an operation upon the operands dependent upon an operation specified by a byte instruction, thereby producing an intermediate result;

adder logic coupled to receive the intermediate result and configured to perform an addition operation upon the intermediate result, thereby producing a sum and a sum+1; and

post-processing logic coupled to receive the sum and sum+1 and configured to perform an operation upon the sum and sum+1 dependent upon the operation specified by a byte instruction, thereby producing a result.

9. The byte execution unit as recited in claim 8, wherein the byte instruction specifies either a count ones in bytes operation, an average bytes operation, an absolute differences of bytes operation, or a sum bytes into halfwords operation.

10. The byte execution unit as recited in claim 8, wherein the pre-processing logic and the post-processing logic are each coupled to receive control signals indicative of the operation specified by the byte instruction.

11. The byte execution unit as recited in claim 8, wherein the pre-processing logic comprises population counter logic coupled to receive the operands and configured to produce population output signals indicative of numbers of logic ones in portions of the operands.

12. The byte execution unit as recited in claim 8, wherein the pre-processing logic comprises compressor logic coupled to receive the operands and configured to perform a compression function.

13. The byte execution unit as recited in claim 8, wherein the post-processing logic comprises end-around carry logic configured to perform an end-around carry function.

14. The byte execution unit as recited in claim 8, wherein the post-processing logic is configured to perform bit shift operations.

15. A logic system, comprising:

compressor logic coupled to receive an 4n-bit operand and configured to perform a compression operation upon the operand, thereby producing a plurality of compressor output signals; and

adder logic coupled to receive the compressor output signals and configured to perform an addition operation upon the compressor output signals, thereby producing an (n+2)-bit result.

16. The logic system as recited in claim 15, wherein the addition operation comprises an (n+1)-bit addition operation.

17. The logic system as recited in claim 16, wherein the adder logic comprises an n-bit adder.

18. The logic system as recited in claim 17, wherein n = 8.

19. A byte execution unit, comprising:

a plurality of byte units, wherein each byte unit comprises:

a plurality of population counters each coupled to receive a portion of a first operand and configured to produce a population output signal indicative of a number of logic ones in the corresponding portion of the first operand;

a first compressor unit coupled to receive a portion of the first operand and configured to produce a first plurality of compressor output signals dependent upon the first operand;

a second compressor unit coupled to receive a portion of the second operand and configured to produce a second plurality of compressor output signals dependent upon the second operand;

adder input multiplexer logic coupled to receive the population output signals and the first and second pluralities of compressor output signals as data input signals, and a first plurality of control signals, and configured to produce a portion of the data input signals as output signals dependent upon the first plurality of control signals;

adder logic coupled to receive the output signals produced by the adder input multiplexer logic and configured to produce a plurality of adder output signals dependent upon the output signals produced by the adder input multiplexer logic; and

result multiplexer logic coupled to receive the adder output signals as data input signals, and a second plurality of control signals, and configured to produce a portion of the data input signals as a result signal dependent upon the second plurality of control signals;

wherein the byte execution unit is coupled to receive byte instruction information, and wherein the first and second pluralities of control signals are indicative of the byte instruction information, and wherein the byte instruction information specifies either a count ones in bytes operation, an average bytes operation, an absolute differences of bytes operation, or a sum bytes into halfwords operation.

20. The byte execution unit as recited in claim 19, wherein the first and second operands each comprise a plurality of bits, and wherein the bits of the first and second operands are grouped to form a plurality of corresponding 8-bit bytes.

21. The byte execution unit as recited in claim 20, wherein the first and second operands each comprise 128 bits, and wherein the bits of the first and second operands are grouped to form 16 corresponding bytes.

22. The byte execution unit as recited in claim 20, wherein in the event the byte instruction information specifies the count ones in bytes operation, the result signal is indicative of a number of logic one bits in each of the bytes of the first operand.

23. The byte execution unit as recited in claim 20, wherein in the event the byte instruction information specifies the average bytes operation, the result signal is indicative of averages of corresponding bytes of the first and second operands.

24. The byte execution unit as recited in claim 20, wherein in the event the byte instruction information specifies the absolute differences of bytes operation, the result signal is indicative of an absolute value of a result of subtraction operations wherein bytes of the first operand are subtracted from the corresponding bytes of the second operand.

25. The byte execution unit as recited in claim 20, wherein in the event the byte instruction information specifies the sum bytes into halfwords operation, the result signal is indicative of sums of values of consecutive bytes of the first and second operands.

26. The byte execution unit as recited in claim 20, wherein the first compressor unit of one of the byte units is coupled to receive a 32-bit portion A[0:31] of the first operand, and wherein the first plurality of compressor output signals produced by the second compressor unit comprises output signals F2[0:7], F2[8], and F3[0:7], and wherein the F2[0] signal conveys a carry value resulting from an addition operation A[0] + A[8] + A[16], and wherein the F2[1:8] signal conveys a sum vector, and wherein the F2[8] signal conveys a sum value resulting from an addition operation A[7] + A[15] + A[23] + A[31], and wherein the F3[0:7] signal conveys a carry vector.

27. The byte execution unit as recited in claim 20, wherein the second compressor unit of one of the byte units is coupled to receive a portion B[0:31] of the second operand, and wherein the second plurality of compressor output signals produced by the second compressor unit comprises output signals F0[0:7], F0[8], and F1[0:7], and wherein the F0[0] signal conveys a carry value resulting from an addition operation B[0] + B[8] +

B[16], and wherein the F0[1:8] signal conveys a sum vector, and wherein the F0[8] signal conveys a sum value resulting from an addition operation B[7] + B[15] + B[23] + B[31], and wherein the F1[0:7] signal conveys a carry vector.

28. The byte execution unit as recited in claim 20, wherein the adder logic comprises a plurality of 8-bit compound adders.

29. A data processing system, comprising:

a memory system comprising a byte instruction, wherein the byte instruction specifies either a count ones in bytes operation, an average bytes operation, an absolute differences of bytes operation, or a sum bytes into halfwords operation; and

a processor coupled to the memory system and configured to fetch and execute instructions from the memory system, wherein the processor comprises:

a byte execution unit coupled to receive byte instruction information and two operands and configured to perform an operation specified by the byte instruction information upon at least one of the two operands, thereby producing a result.

30. The data processing system as recited in claim 29, wherein each of the two operands comprises a plurality of bits, and wherein the bits of the two operands are grouped to form a plurality of corresponding 8-bit bytes.

31. The data processing system as recited in claim 30, wherein each of the two operands comprises 128 bits, and wherein the bits of the two operands are grouped to form 16 corresponding bytes.